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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,521	11/24/2003	Akira Takeda	S004-5169	5322
7590	05/18/2005		EXAMINER	NGUYEN, HIEP
ADAMS & WILKS 50 Broadway 31st Floor New York, NY 10004			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/721,521	TAKEDA ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 02 March 2005.

2a) This action is FINAL.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1,2,4,5 and 7-12 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1,2,4,5 and 7-12 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

The amendment filed on 03-02-05 has been received and entered in the case. New ground of rejections necessitated by the amendment and newly added claims is set forth below.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations “a control circuit” in claims 2, 9 and 10, “a single reference voltage generator” in claims 4 and 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2, 4, 9 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The recitations “a control circuit” in claims 2, 9 and 10, “a single reference voltage generator” in claims 2 and 9 are not described in the specification. The specification fails to describe the functioning of the “control circuit” as recited in claim 2, 9 and 10 such as “adjust at least one of the first reference voltage...” in claims 2 and 9; “adjust a temperature characteristic...” in claim 10.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Regarding claim1, the recitation “so that noise components of the reference voltages are in phase to reduce noise during adjustment of an offset voltage between the input terminals” is indefinite because it is not clear how the offset voltage can be adjusted by two in phase noise components.

Claims 2, 7 and 9-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 2 and 9, the recitation “**a control circuit for adjusting** at least one of the first reference voltage and the second reference voltage” is indefinite because it is misdescriptive. As understood by the examiner, the control circuit comprises a voltage follower and resistors (161,162) in figure 1 of the present application. There is **no control circuit for adjustment** seen because voltage (Vref) is a **fixed voltage**. The Applicant is requested to point out the “a control circuit” in the drawing. The recitation “... so that a voltage difference between the first reference voltage and the second reference voltage **coincides** in phase with **an offset voltage** between the first input terminal and the second input terminal” is indefinite because it is confusing. It is not clear how the difference between the first reference voltage and the second reference voltage can “coincide” in phase with an

offset voltage. Clear explanation is required. Note that as understood by the examiner, the reference voltage generator generates two reference voltages that are in phase (noise). In claim 9, it is not clear as to the “a single reference voltage generator” is the same or different from the “a control circuit” because they both generate reference voltages. The Applicant is requested to point out the “single reference voltage generator” and the “control circuit” in the drawing.

Claims 7, 8, 10 and 12 are indefinite because of the technical deficiencies of claims 1, 2 and 9.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 4, 5, and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, figure 2 in view of Motegi et al. (US Pat. 6,653,999).

Regarding claim 1, the prior art, figure 2 shows a switched capacitor amplifier circuit, comprising: a pair of input terminals (141) and (142), a pair of capacitors (101, 102), a pair of reference voltage terminals (111, 112). The prior art does not show that “the reference voltage terminals being connected to respective switch circuits so that noise components of the reference voltages are in phase to reduce noise during adjustment of an offset voltage between the input terminals”. In other word, the prior art does not show that the reference voltage generator that generates the reference voltages comprises a voltage follower receiving a reference voltage and a resistor network for generating two reference voltages. Figure 1 of Motegi shows a reference voltage generator comprising a voltage follower (113) coupled to a resistor network (R1) for generating reference voltages. Therefore, it would have been obvious to an artisan having skills in the art at the time the invention was made to replace the reference voltage generator circuit of the prior art with the reference generator circuit taught by Motegi that has fewer active elements for reducing the size of the circuit and for

minimizing the production cost. Note that the reference generator circuit of Motegi has a single voltage follower (113) generating a reference voltage (VLCDO). This voltage is divided by a resistive network for supplying two other reference voltages (VLCD1, VLCD2). The reference voltage generator of Motegi relies only on one single reference voltage (VLCDO) and a voltage divider circuit comprising resistive components. As a result, the noises of the reference voltages (or the reference voltages) have the same phase. Thus, noise components of the reference voltages of the reference voltage generator taught by Motegi are in phase to “reduce noise during adjustment of an offset voltage between the input terminals”.

Regarding claim 2, the prior art shows a switch capacitor circuit amplifier circuit comprising: first and second input terminals (141, 142), first and second capacitors (101, 102), an op-amp, first and second reference voltage terminals coupled to the left sides of capacitors (101) and (102); “a control circuit” comprising two voltage followers supplying reference voltages (Vref1, Vref2). The prior art does not show that the “control circuit” generates two reference signals that are in phase. Figure 1 of Motegi shows a reference voltage generator comprising a voltage follower (113) coupled to a resistor network (R1) for generating reference voltages. Therefore, it would have been obvious to an artisan having skills in the art at the time the invention was made to replace the reference voltage generator circuit of the prior art with the reference generator circuit taught by Motegi that has fewer active elements for reducing the size of the circuit and for minimizing the production cost. Note that the reference generator circuit of Motegi has a single voltage follower (113) generating a reference voltage (VLCDO). This voltage is divided by a resistive network for supplying two other voltages (VLCD1, VLCD2). The reference voltage generator of Motegi relies only on one single reference voltage (VLCDO) and a voltage divider circuit comprising resistive components. As a result, the noises of the reference voltages (or the reference voltages) have the same phase. Thus, noise components of the reference voltages of the reference voltage generator taught by Motegi are in phase to “reduce noise during adjustment of an offset voltage between the input terminals”.

Regarding claims 4, 9 and 10, the circuit of the combination of the prior art and the circuit of Motegi are identical to the circuit of figure 1 of the present application. The combination shows a switched capacitor amplifier circuit comprising; an operational

amplifier, first to sixth capacitors and first to twelve switches connected as described in claim 4; a single reference voltage generator (element 113 of Motegi) that generates first and second reference voltages. In claims 9 and 10, the “control circuit” taught by Motegi “adjust” the first and second reference voltages so that they both in phase.

Claims 5, 7, 8, 11 and 12 are rejected under 103(a). The recitation “An electronic device” is merely intended use thus; it does not further limit the limitations of the claim. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Therefore, this limitation has not been given patentable weight.

#### *Response to Arguments*

In page 20 and 21, the Applicant argues that “the crystal driving disclosed by Motegi does not correspond either in structure or function to a switched capacitor amplifier circuit. That is correct. The circuit of figure 1 of Motegi is merely a reference voltage generator circuit although it is labeled the “integrated circuit for driving liquid crystal”. The circuit of figure 1 divides reference voltage (VLCDO) into other reference voltages (VLCDO, col. 1 lines 31-33) with a resistor network. The prior art, figure 2 of the present application includes all the limitations of claim 1 except for the limitation that the reference generator circuit of the prior art comprises two different reference voltages and two voltage followers while the reference voltage generator circuit of figure 1 comprises one voltage follower and a voltage divider. Figure 1 of Motegi shows a reference voltage generator (labeled as integrated circuit for driving liquid crystal). This circuit is simply a reference voltage generator circuit thus, it “does not correspond either in structure or function to a switched capacitor amplifier circuit” of the present application. The circuit of Motegi has an advantage over the reference voltage generator circuit of the prior art which comprises two different reference voltage sources and two different voltage followers. Therefore, it is proper to replace the complicate reference voltage generator circuit of the prior art with the simple reference voltage generator circuit taught by Motegi for cost saving because the circuit of Motegi includes less active components. Another advantage of the circuit of Motegi is that while the reference voltage

generating circuit of the prior art relies on two different reference voltages and two different voltage followers, the noises of the reference voltages can be from different voltage sources thus, the noises have difference phases. The reference voltage generator circuit taught by Motegi relies only on one single reference voltage (VLCDO) and a voltage divider circuit comprising resistive components. As a result, the noises of the reference voltages of Motegi have the same phase.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

05-11-05

*Mr*



TUAN T. LAM  
PRIMARY EXAMINER